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<u>L13</u>	L9 and page	0	<u>L13</u>
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<u>L11</u>	L9 and (partition\$ or section\$)	1	<u>L11</u>
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<u>L9</u>	L8 and data near record	2	<u>L9</u>
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<u>L7</u>	L5 and garbage near manag\$	1	<u>L7</u>
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<u>L4</u>	garbage near3 manag\$	361	<u>L4</u>
<u>L3</u>	((707/205)!.CCLS. )	562	<u>L3</u>
<u>L2</u>	((707/204)!.CCLS. )	659	<u>L2</u>
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Terms	Documents
L29 and (rank\$ or weight\$) near3 data near3 records	23

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<u>L30</u>	L29 and (rank\$ or weight\$) near3 data near3 records	23	<u>L30</u>
<u>L29</u>	L28 and key	6743	<u>L29</u>
<u>L28</u>	L27 and data near3 records	11263	<u>L28</u>
<u>L27</u>	(database or data with base)and manag\$ with system	62428	<u>L27</u>
<u>L26</u>	((711/130)!.CCLS.) )	219	<u>L26</u>
<u>L25</u>	((711/129)!.CCLS.) )	245	<u>L25</u>
<u>L24</u>	((711/117)!.CCLS.) )	319	<u>L24</u>
<u>L23</u>	((711/160)!.CCLS.) )	155	<u>L23</u>
<u>L22</u>	((711/113)!.CCLS.) )	651	<u>L22</u>
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<u>L15</u>	((707/8 )!.CCLS. )	639	<u>L15</u>
<u>L14</u>	L10 and databse adj manag\$	1	<u>L14</u>
<u>L13</u>	L12 and error near4 section\$2	3	<u>L13</u>
<u>L12</u>	L10 and stor\$ near2 data near2 record	488	<u>L12</u>
<u>L11</u>	L10 and stor\$	1899	<u>L11</u>
<u>L10</u>	L9 and key	1903	<u>L10</u>
<u>L9</u>	L8 and data near4 records	2516	<u>L9</u>
<u>L8</u>	L7 and sections	6426	<u>L8</u>
<u>L7</u>	(database or data with base) near2 manag\$	23022	<u>L7</u>
<u>L6</u>	L5 and rank\$	11	<u>L6</u>
<u>L5</u>	L4 and retriev\$	63	<u>L5</u>
<u>L4</u>	L3 and page\$2	64	<u>L4</u>
<u>L3</u>	L2 and control adj5 program	78	<u>L3</u>
<u>L2</u>	L1 and primary near4 stor\$	130	<u>L2</u>
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L6: Entry 10 of 11

File: USPT

Oct 26, 1982

US-PAT-NO: 4356550

DOCUMENT-IDENTIFIER: US 4356550 A

TITLE: Multiprocessor system

DATE-ISSUED: October 26, 1982

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Katzman; James A.	San Jose	CA		
Bartlett; Joel F.	Palo Alto	CA		
Bixler; Richard M.	Sunnyvale	CA		
Davidow; William H.	Atherton	CA		
Despotakis; John A.	Pleasanton	CA		
Graziano; Peter J.	Los Altos	CA		
Green; Michael D.	Los Altos	CA		
Greig; David A.	Cupertino	CA		
Hayashi; Steven J.	Cupertino	CA		
Mackie; David R.	Ben Lomond	CA		
McEvoy; Dennis L.	Scotts Valley	CA		
Treybig; James G.	Sunnyvale	CA		
Wierenga; Steven W.	Sunnyvale	CA		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Tandem Computers Incorporated	Cupertino	CA			02

APPL-NO: 06/ 147305 [PALM]

DATE FILED: May 6, 1980

## PARENT-CASE:

This application is a division of parent Application Ser. No. 721,043 filed Sept. 7, 1976, now U.S. Pat. No. 4,228,496, and entitled "Multiprocessor System" and claims the benefit of the filing date of the parent Application.

INT-CL: [03] G06F 11/20

US-CL-ISSUED: 364/200

US-CL-CURRENT: 714/14; 714/22

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 371/66

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected

Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>3827030</u>	July 1974	Seipp	364/900
<input type="checkbox"/>	<u>3859638</u>	January 1975	Hume, Jr.	365/228
<input type="checkbox"/>	<u>4004283</u>	January 1977	Bennett et al.	364/200
<input type="checkbox"/>	<u>4015243</u>	March 1977	Kurpanek et al.	364/200
<input type="checkbox"/>	<u>4048672</u>	September 1977	Seiden et al.	364/200
<input type="checkbox"/>	<u>4050096</u>	September 1977	Bennett	364/200

ART-UNIT: 232

PRIMARY-EXAMINER: Thomas; James D.

ASSISTANT-EXAMINER: Eng; David Y.

ATTY-AGENT-FIRM: Feix; Donald C. Eakin; James E.

ABSTRACT:

A multiprocessor system, the kind in which two or more separate processor modules are interconnected for two power supplies, provides the entire power for the device controller in the event the other power supply fails. The distributed power supply system permits any processor module or device controller to be powered down so that on-line maintenance can be performed in a power-off condition while the rest of the multiprocessor system is on-line and functional.

The multiprocessor system includes a memory system in which the memory of each processor module is divided into four logical address areas--user data, system data, user code and system code. The memory system includes a map which translates logical addresses to physical addresses and which coacts with the multiprocessor system to bring pages from secondary memory into primary main memory as required to implement a virtual memory system. The map also provides a protection function. It provides inherent protection among users in a multiprogramming environment, isolates programs from data and protects system programs from the actions of user program. The map also provides a reference history information for each logical page as an aid to efficient memory management by the operating system.

The multiprocessor system includes in the memory of each processor module an error detection and correction system which detects all single bit and double bit errors and which corrects all single bit errors in semiconductor memory storage.

7 Claims, 42 Drawing figures

**WEST**☐ **Generate Collection** **Print**

L6: Entry 8 of 11

File: USPT

Mar 29, 1983

US-PAT-NO: 4378588

DOCUMENT-IDENTIFIER: US 4378588 A

TITLE: Buffer control for a data path system

DATE-ISSUED: March 29, 1983

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Katzman; James A.	San Jose	CA		
Bartlett; Joel F.	Palo Alto	CA		
Bixler; Richard M.	Sunnyvale	CA		
Davidow; William H.	Atherton	CA		
Despotakis; John A.	Pleasanton	CA		
Graziano; Peter J.	Los Altos	CA		
Green; Michael D.	Los Altos	CA		
Greig; David A.	Cupertino	CA		
Hayashi; Steven J.	Cupertino	CA		
Mackie; David R.	Ben Lomond	CA		
McEvoy; Dennis L.	Scotts Valley	CA		
Treybig; James G.	Sunnyvale	CA		
Wierenga; Steven W.	Sunnyvale	CA		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Tandem Computers Incorporated	Cupertino	CA			02

APPL-NO: 06/ 147091 [PALM]

DATE FILED: May 6, 1980

## PARENT-CASE:

This application is a division of parent application Ser. No. 721,043 filed Sept. 7, 1976 (now a U.S. Pat. No. 4,228,496) and entitled "Multiprocessor System" and claims the benefit of the filing date of the parent application.

INT-CL: [03] G06F 13/00, G11C 9/00

US-CL-ISSUED: 364/200

US-CL-CURRENT: 710/57; 709/234

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 235/92PE, 235/132R, 360/51, 360/73

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

**Search Selected****Search ALL**

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>3059221</u>	October 1962	Page et al.	364/900
<input type="checkbox"/>	<u>3292156</u>	December 1966	Stochel	364/900
<input type="checkbox"/>	<u>3836891</u>	September 1974	McDaniel	364/900
<input type="checkbox"/>	<u>4040026</u>	August 1977	Gernelle	364/200
<input type="checkbox"/>	<u>4040027</u>	August 1977	Van Es et al.	364/900

ART-UNIT: 237

PRIMARY-EXAMINER: Chan; Eddie P.

ATTY-AGENT-FIRM: Feix; Donald C.

## ABSTRACT:

A datapath system and protocol is disclosed in which data is transferred between a computer memory and one or more peripheral devices through device controllers, each of which includes a buffer, through periodic connection of the device controller to the channel. The system and protocol are structured to permit multiple device controllers to cooperatively interact on a single channel, without direct communication between device controllers. Each device controller monitors the level of stress on its buffer and at appropriate times presents a reconnect request to the channel, together with indica for permitting the channel to determine the priority of a particular request relative to other reconnect requests. The times at which a reconnect signal should be presented are determined by monitoring the level of information storage in the buffer and relating that level to a threshold level; both overfilling and overemptying are prevented. The threshold level can be varied in accordance with a criteria which makes allowance for the number and combination of device controllers attached to the channel; and is set such that the remaining space in the buffer is sufficient to allow the buffer to transfer data to or from the associated peripheral device, at the rate demanded by that peripheral device, long enough to allow the channel to connect to one lower priority device controller, and all higher priority device controllers. The threshold level and buffer size are also set such that, after a reconnect, the buffer is capable of transferring data to or from the associated peripheral device, at the rate demanded by the peripheral, long enough for the channel to reconnect to all lower priority device controllers, to ensure that all device controllers, no matter the priority, are allowed access to the channel. The invention has broad application, but is particularly well-suited to fault tolerant computing systems.

6 Claims, 42 Drawing figures



**WEST**☐ **Generate Collection** **Print**

L30: Entry 22 of 23

File: USPT

Apr 9, 1985

US-PAT-NO: 4510567

DOCUMENT-IDENTIFIER: US 4510567 A

TITLE: Qualifying and sorting file record data

DATE-ISSUED: April 9, 1985

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chang; Philip Y.	Austin	TX		
McInroy; John W.	Austin	TX		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE	CODE
International Business Machines Corp.	Armonk	NY				02

APPL-NO: 06/ 264797 [PALM]

DATE FILED: May 18, 1981

INT-CL: [03] G06F 7/00, G06F 7/24

US-CL-ISSUED: 364/300

US-CL-CURRENT: 707/7

FIELD-OF-SEARCH: 364/2MSfile, 364/9MSfile

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

**Search Selected****Search ALL**

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>3872442</u>	March 1975	Boles et al.	364/200
<input type="checkbox"/>	<u>4031520</u>	June 1977	Rohner	364/900
<input type="checkbox"/>	<u>4080651</u>	March 1978	Cronshaw et al.	364/200
<input type="checkbox"/>	<u>4101968</u>	July 1978	Florence	364/900
<input type="checkbox"/>	<u>4209845</u>	June 1980	Berger et al.	364/900
<input type="checkbox"/>	<u>4393470</u>	July 1983	Miarn	364/200
<input type="checkbox"/>	<u>4417321</u>	November 1983	Chang et al.	364/900

## OTHER PUBLICATIONS

Software Tools in Pascal, Kernigan and Plauges published by Bell Labs. Inc. 1981  
--Chapter 4.An Operator Orientated Data Base Management System by J. Shapiro published in  
Kilobaud, Mar. 1980, p. 84.

Data Base Management by K. Widelitz published in Kilobaud, May 1979, p. 54.  
Sorting Routines by Andrew J. Rerko, Kilobaud, Apr. 1977, pp. 34-36.

ART-UNIT: 237

PRIMARY-EXAMINER: Shaw; Gareth D.

ASSISTANT-EXAMINER: Mills; John G.

ATTY-AGENT-FIRM: Meier; Harold E.

ABSTRACT:

Record data on a disk file is sorted in a text/data processor by means of an algorithm that transfers such records on the basis of rank to a sort buffer on the basis of qualifying criteria. Each qualified file record is compared with the lowest ranked record previously transferred and located in the sort buffer. When a higher ranked record is identified it is transferred into the buffer at a location based on qualification. Lower ranked records are deleted from the sort buffer if space does not permit the storing of such records within the space available. When the sort buffer has been loaded with the highest ranked records remaining in the disk file without overflowing the buffer is unloaded to an output device. The sort program recycles through a subsequent pass again transferring the highest ranked remaining records into the sort buffer. To minimize recycle time, a presort algorithm is run to set record identifying bits in a bit map section of the sort buffer. Each time the contents of the sort buffer is output the record identifying bits for the records in the sort buffer are reset to a second state. The second state of a record identifying bit indicates that that record will not be considered for future passes through the sort routine.

8 Claims, 8 Drawing figures

**WEST****End of Result Set**☐ **Generate Collection** **Print**

L9: Entry 2 of 2

File: USPT

Oct 31, 1995

US-PAT-NO: 5463770

DOCUMENT-IDENTIFIER: US 5463770 A

TITLE: System and method for controlling data storage in a data processing system in which objects generated within a lower level language program are associated with memory slots allocated to another program

DATE-ISSUED: October 31, 1995

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Todd; Stephen J. P.	Winchester			GB2

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE	CODE
International Business Machines Corporation	Armonk	NY			02	

APPL-NO: 08/ 400301 [PALM]

DATE FILED: March 6, 1995

## PARENT-CASE:

This application is a continuation of application Ser. No. 08/095,633, filed Jul. 21, 1993, now abandoned.

## FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
GB	9215597	July 22, 1992

INT-CL: [06] G06 F 13/00, G06 F 12/00

US-CL-ISSUED: 395/600; 395/650, 395/700, 364/DIG.1, 364/281.1, 364/284, 364/239.9, 364/245

US-CL-CURRENT: 707/206; 709/320

FIELD-OF-SEARCH: 395/600, 395/425, 395/700

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5189733</u>	February 1993	Bennett et al.	395/425
<input type="checkbox"/>	<u>5202971</u>	April 1993	Henson et al.	395/425
<input type="checkbox"/>	<u>5274804</u>	December 1993	Jackson et al.	395/600
<input type="checkbox"/>	<u>5315709</u>	May 1994	Alston, Jr. et al.	395/600
<input type="checkbox"/>	<u>5321834</u>	June 1994	Weiser et al.	395/600
<input type="checkbox"/>	<u>5392432</u>	February 1995	Engelstad et al.	395/600
<input type="checkbox"/>	<u>5398334</u>	March 1995	Topka et al.	395/600

## OTHER PUBLICATIONS

Vogt, "Storage Organisation in Object-Oriented Systems: A Survey", Informationstechnik It. vol. 33, No. 4, Aug. 1991, Munchen Br, pp. 208-219. No English translation.

Ichiyoshi et al., "A New External Reference Management and Distributed Unification for KL1". New Generation Computing. vol. 7, No. 2/3, 1990, Berlin DE pp. 159-177.

Foster, "A Multicomputer Garbage Collector for a Single-Assignment Language", International Journal of Parallel Programming, vol. 18, No. 3, Jun. 1989, New York US, pp. 181-203.

ART-UNIT: 236

PRIMARY-EXAMINER: Chan; Eddie P.

ATTY-AGENT-FIRM: Truelson; Roy W. Bussan; Matthew J.

## ABSTRACT:

A data processing system of the type in which a first program interacts with a second lower level language program is provided, the system includes a lower level language subroutine for generating objects within the second program, a memory for storing the objects, and an interface, object surrogates and surrogate references for associating the objects with one or more slots allocated to the first program. The interface is generated between the first and second programs by the first program, the interface residing within the first program. The object surrogates are then contained within the interface, each object surrogate containing an identifier for a given object. To associate one or more of the slots with a particular object surrogate, the surrogate references identifying the object surrogates are stored by the first program in those slots. During operation of the first program slots may be redefined by erasing old surrogate references and replacing them with different ones. When an object surrogate is no longer associated by any surrogate reference with any of the slots, then a high level language garbage collector informs the second program. By employing such an approach the data processing system is able to automatically keep track of objects, releasing the user from the burden of having to set up L.L.L. checking routines of his own, and further enabling the system to make much more efficient use of available memory.

10 Claims, 4 Drawing figures

**WEST**

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L14: Entry 14 of 15

File: USPT

Mar 27, 1990

US-PAT-NO: 4912629

DOCUMENT-IDENTIFIER: US 4912629 A

TITLE: Real-time garbage collection for list processing using restructured cells for increased reference counter size

DATE-ISSUED: March 27, 1990

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shuler, Jr.; Robert L.	Friendswood	TX		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE	CODE
The United States of America as represented by the Administrator of the	Washington DC					06

APPL-NO: 06/ 878916 [PALM]

DATE FILED: June 26, 1986

INT-CL: [04] G06F 9/00, G06F 12/00

US-CL-ISSUED: 364/200; 364/281.1, 364/280

US-CL-CURRENT: 707/206

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 364/300

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected

Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4016545</u>	April 1977	Lipovski	364/900
<input type="checkbox"/>	<u>4121286</u>	October 1978	Venton et al.	364/200
<input type="checkbox"/>	<u>4193115</u>	March 1980	Albus	
<input type="checkbox"/>	<u>4215397</u>	July 1980	Hom	364/101
<input type="checkbox"/>	<u>4432057</u>	February 1984	Daniell et al.	364/300
<input type="checkbox"/>	<u>4435752</u>	March 1984	Winkelman	364/200
<input type="checkbox"/>	<u>4435766</u>	March 1984	Haber et al.	364/300
<input type="checkbox"/>	<u>4447875</u>	May 1984	Bolton et al.	364/200
<input type="checkbox"/>	<u>4463424</u>	July 1984	Mattson et al.	364/200
<input type="checkbox"/>	<u>4502118</u>	February 1985	Hagenmaier et al.	364/200
<input type="checkbox"/>	<u>4558413</u>	December 1985	Schmidt et al.	364/300
<input type="checkbox"/>	<u>4695949</u>	September 1987	Thatte et al.	364/200
<input type="checkbox"/>	<u>4716524</u>	December 1987	Oxley et al.	364/200
<input type="checkbox"/>	<u>4758944</u>	July 1988	Bartley et al.	364/200
<input type="checkbox"/>	<u>4775932</u>	October 1988	Oxley et al.	364/200

## OTHER PUBLICATIONS

"Dynamic Page Reference Counter," IBM Technical Disclosure Bulletin, vol. 21, No. 8, Jan. 1979, J. N. McCauley and J. A. Wingert, (pp. 3139-3140).  
"Efficient Real-Time Garbage Collection for LISP," Jun. 27, 1985, Robert L. Shuler, Jr.

"Performance Analysis of On the Fly Garbage Collection," Communications of the ACM, vol. 27, No. 11, Nov. 1984, Tim Hickey and Jacques Cohen, (pp. 1143-1154).

"Garbage Collection of Linked Data Structures," ACM Computing Surveys, vol. 13, No. 3, Sep. 1981, Jacques Cohen, (pp. 341-367).

"A Real-Time Garbage Collector Based on the Lifetimes of Objects," Communications of the ACM, vol. 26, No. 6, Jun. 1983, Henry Lieberman and Carl Hewitt.

"LISP," 2nd Ed., Addison-Wesley, 1984, Patrick Henry Winston and Berthold Klaus Paul Horn, (p. 141).

"An Efficient Machine-Independent Procedure for Garbage Collection in Various List Structures," Communications of the ACM, vol. 10, No. 8, Aug. 1967, H. Schorr and W. M. Waite, (pp. 501-506).

ART-UNIT: 237

PRIMARY-EXAMINER: Shaw; Gareth D.

ASSISTANT-EXAMINER: Kriess; Kevin A.

ATTY-AGENT-FIRM: Schlorff; Russell E. Manning; John R. Fein; Edward K.

## ABSTRACT:

In a list processing system, small reference counters are maintained in conjunction with memory cells for the purpose of identifying memory cells that become available for re-use. The counters are updated as references to the cells are created and destroyed, and when a counter of a cell is decremented to logical zero the cell is immediately returned to a list of free cells. In those cases where a counter must be incremented beyond the maximum value that can be represented in a small counter, the cell is restructured so that the additional reference count can be represented. The restructuring involves allocating an additional cell, distributing counter, tag, and pointer information among the two cells, and linking both cells appropriately into the existing list structure.

22 Claims, 9 Drawing figures